MC141563

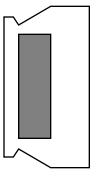
LCD Segment (Column) Driver
CMOS

The MC141563 is a high volt, high MUX passive LCD segment driver. It is a CMOS LCD driver chip which consists of 80-channel segment driving outputs for a high MUX (up to 300 MUX) large dot matrix passive LCD panel.

This chip interfaces with 4-bit or 8-bit data bus with bidirectional shift capability. The 28 V high voltage output driving cells can be controlled by low voltage (3.0 Volts) logic input.

The MC141563 will provide the best performance in combination with the MC141562 (common driver).

- Operating Supply Voltage Range -
  Control Logic, Shift Register (VDD): 2.7V to 5.5V
  Segment Drivers (VLCD): 10 V to 28 V
- Operating Temperature Range: -20 to 70˚C
- 80 LCD Segment Driving Outputs.
- Driving Duty Cycle (MUX) : 1/64 to 1/300.
- Bi-directional Shift Register Data Bus of 4-bit x 20 or 8-bit x 10 Configuration.
- Interchangeable Carry-In / Carry-Out Terminals.
- Left / Right Shift Mode Selection
- Cascadable.
- Maximum Data Clock Frequency = 8.0 MHz
- Available in SLIM TAB (Tape Automated Bonding), 103 pins



MC141563T

TAB

ORDERING INFORMATION

MC141563T	TAB

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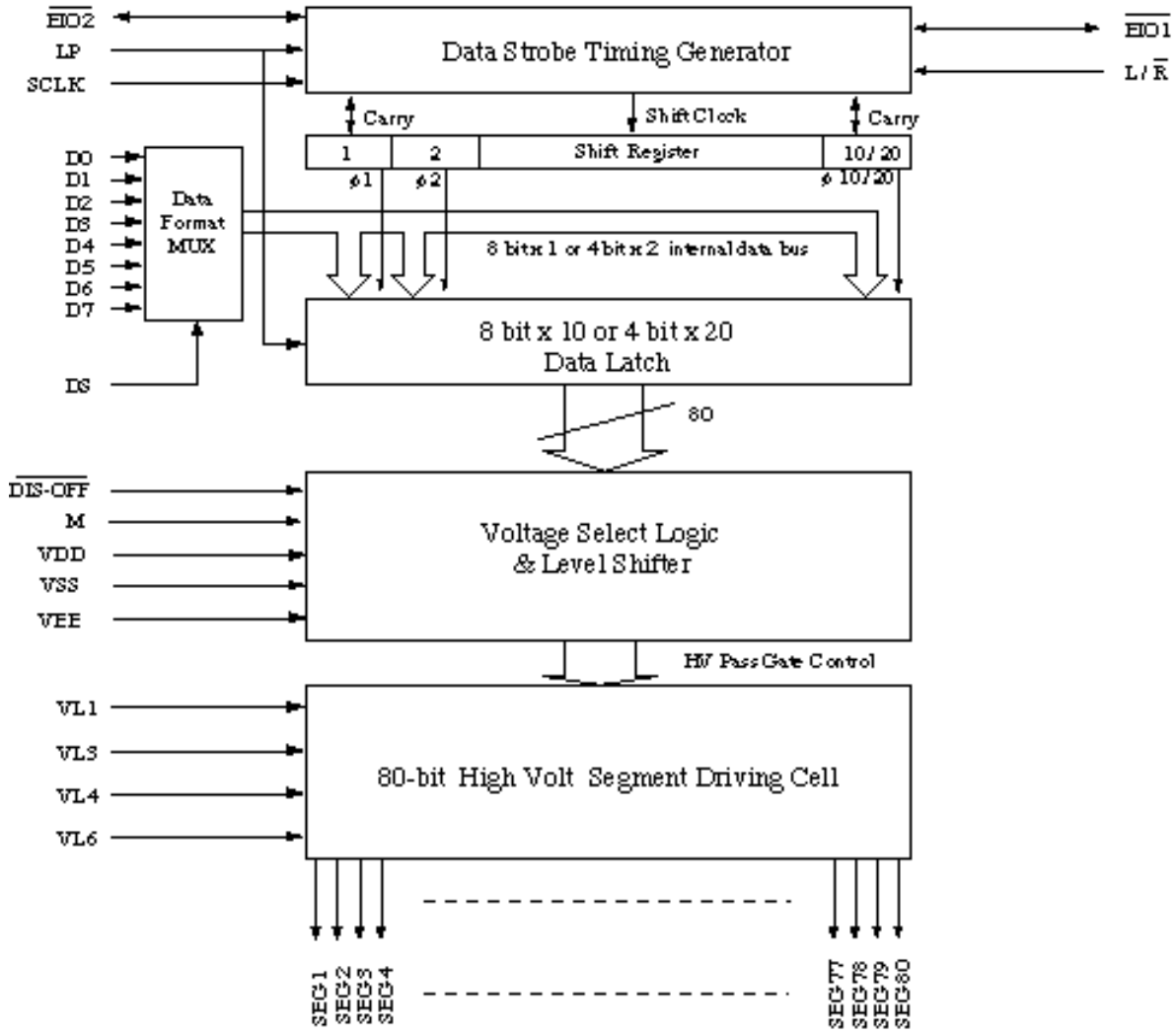
10/96

Figure 1. BLOCK DIAGRAM



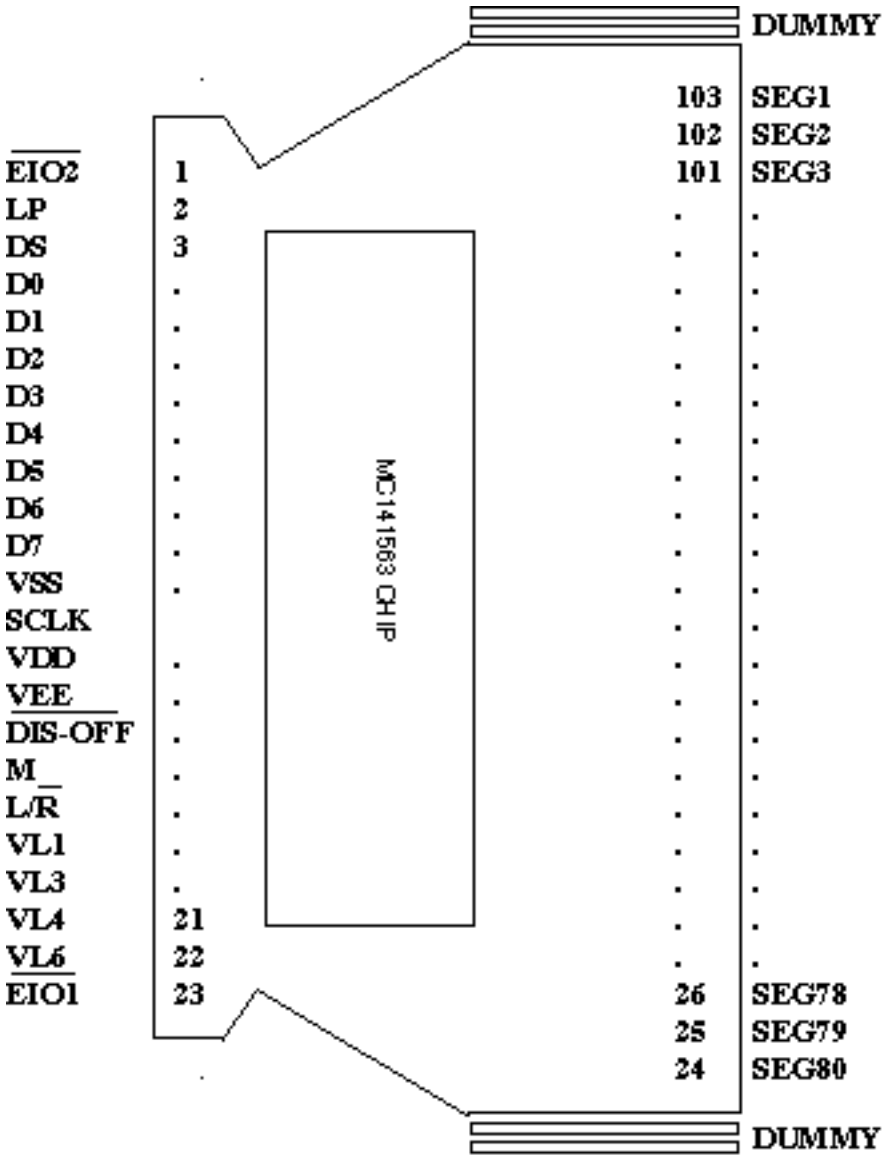


Figure 2. TAB Package Contact Assignment (Copper View)

MAXIMUM RATINGS*(Voltages Referenced to V_{SS}, T_A=25 C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +6.0	V
V_{EE}		-0.3 to -24.0	V
V_{LCD}	DC Supply Voltage (V_{DD} - V_{EE})	V_{DD} to +30	V
V_{Din} V_{Ain}	Input Voltage All Digital Input V_{LCD} Level Input	 V_{SS}-0.3 to V_{DD}+0.3 V_{EE}-0.3 to V_{DD}+0.3	 V V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature Range	-20 to 70	˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A = 25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
 V_{DD} V_{LCD}	Operating Voltage Supply Voltage (reference to V_{SS}) LCD Supply Voltage (V_{DD} - V_{EE})		 2.7 10.0	 - -	 5.5 28.0	V V
 I_{DP} I_{SB}	Supply Current (V_{DD} Pin) Display Mode Standby Mode	V_{DD}=5.5V, V_{EE}=-23V SCLK = 6MHz, LP=15KHz, M=35Hz	 - -	 250 1.5	 600 5.5	 µA µA
 I_{DP} I_{SB}	Supply Current (V_{DD} Pin) Display Mode Standby Mode	V_{DD}=2.7V, V_{EE}=-23V SCLK = 6MHz, LP=15KHz, M=35Hz	 - -	 120 600	 - -	 µA nA
I_{EE}	Supply Current at V_{EE}	No Load	-	30	550	µA
 V_{OL} V_{OH}	Segment Output Voltage VL4,6=V_{EE} VL1,3=V_{DD} SEG1-SEG80	Iload = 100µA	 - V_{DD}-0.3	 - -	 V_{EE}+0.3 -	 V V
V_{OH} V_{OL}	Output High Voltage Output Low Voltage $\overline{EIO1}$, $\overline{EIO2}$	V_{DD}=5.0V, Iload=1mA	V_{DD}-1.0 -	- -	- V_{SS}+1.0	V V
V_{IH} V_{IL}	Input High Voltage Input Low Voltage SCLK, LP, L/$\overline{R}$, $\overline{EIO1}$, $\overline{EIO2}$, D0 to D3, M, $\overline{DIS\text{-}OFF}$		0.7xV_{DD} V_{SS}	- -	V_{DD} 0.2xV_{DD}	V V
I_{in}	Input Current SCLK, LP, L/$\overline{R}$, $\overline{EIO1}$, $\overline{EIO2}$, D0 to D3, M, $\overline{DIS\text{-}OFF}$		-	0.5	1.0	µA
C_{in}	Capacitance SCLK, LP, L/$\overline{R}$, $\overline{EIO1}$, $\overline{EIO2}$, D0 to D3, M, $\overline{DIS\text{-}OFF}$		-	5	10	pF
I_{OHX}, I_{OLX}	Segment Output Current SEG1-SEG80	V_{OH}= V_{DD} - 0.3V, V_{OL}=V_{EE} +0.3V	100	-	-	µA
I_{OHC}, I_{OLC}	Carry Output Current $\overline{EIO1}$, $\overline{EIO2}$	V_{OH}= V_{DD} - 1.0V, V_{OL}=V_{SS} +1.0V	1.0	-	-	mA
R_{ON}	Segment Output Impedance Segment Output Impedance Variance	V_{DD} - V_{EE} =28V, I_{OHX}, I_{OLX}= 100µA	- -	1.5 10	3.0 30	K Ohm %

AC ELECTRICAL CHARACTERISTICS -WRITE CYCLE (V_{DD} =5.0V, V_{SS} = 0V, V_{EE} = -23V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{SUD}	Data (D0-D3) to Shift Clock (SCLK) Set up Time	50	-	-	ns
t_{hD}	Data (D0-D3) to Shift Clock (SCLK) Hold Time	50	-	-	ns
t_{SULP}	Data Latch (LP) to Shift Clock (SCLK) Set up Time	50	-	-	ns
t_{hLP}	Data Latch (LP) to Shift Clock (SCLK) Hold Time	50	-	-	ns
t_{SUS}	Enable Input ($\overline{EIO}$) to Shift Clock (SCLK) Set up Time	20	-	-	ns
t_{SUE}	Shift Clock (SCLK) to Enable Output ($\overline{EIO}$) Set up Time	20	-	-	ns
	Propagation Delay Time				
t_M	Data Latch (LP) to M	-	-	200	ns
t_{PO}	Data Latch (LP) to Segment Output (n) CL = 100pF	-	-	0.5	µs
t_{PM}	M to Segment Output (n) CL = 100pF	-	-	0.5	µs
t_{PLP}	Data Latch (LP) to $\overline{EIO}$ (Output) CL = 50pF	-	-	50	ns
t_{PE}	Shift Clock (SCLK) to $\overline{EIO}$ (Output) CL = 50pF	-	-	50	ns
t_{TLH}	Control Input Rise and Fall Time	-	10	20	ns
t_{THL}	SCLK, LP, M, $\overline{EIO1}$,$\overline{EIO2}$	-	10	20	ns
$t_{SCØ}$	Shift Clock (SCLK) Cycle V_{DD} = 3.0V	125	-	-	ns
t_{SCH}	Shift Clock (SCLK) Pulse Width HIGH	40	-	-	ns
t_{SCL}	Shift Clock (SCLK) Pulse Width LOW	40	-	-	ns
t_{LPH}	Data Latch (LP) Pulse Width HIGH	50	-	-	ns

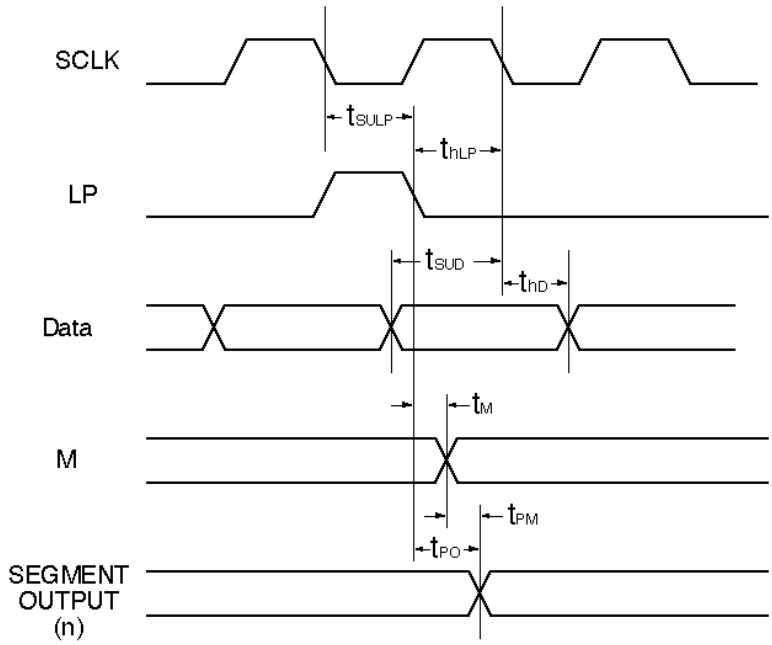


Figure 3. SCLK, LP, Data, M and Segment Output Propagation Delay Timing Diagram

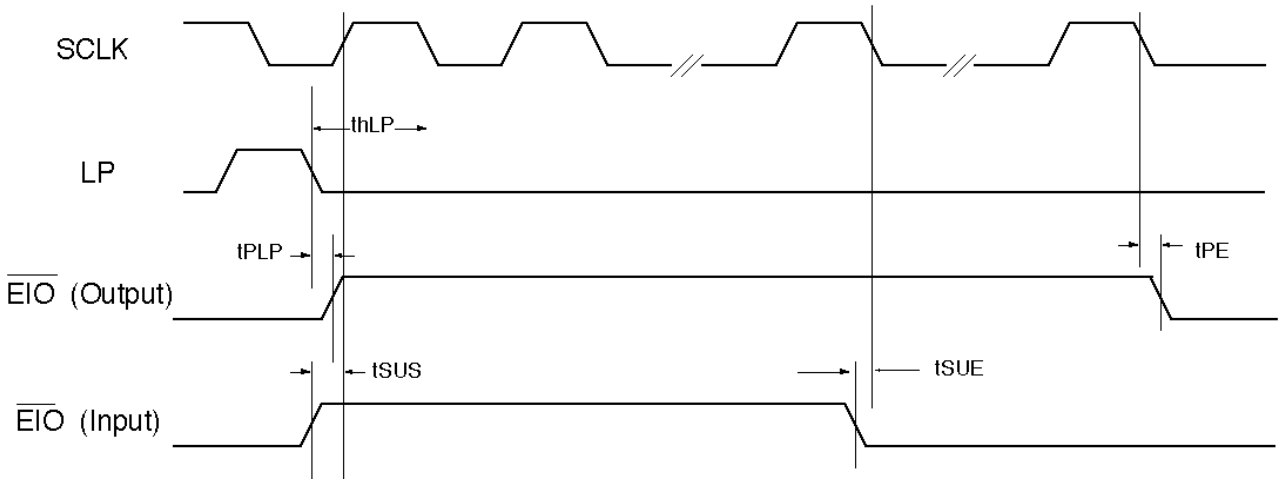


Figure 4. SCLK, LP, EIO (Input/Output) Propagation Delay Timing Diagram

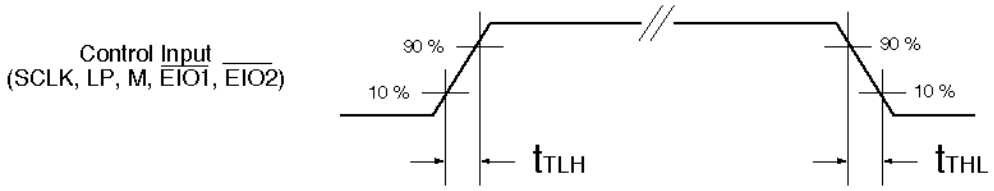


Figure 5. Control Pin Rise and Fall Timing Diagram

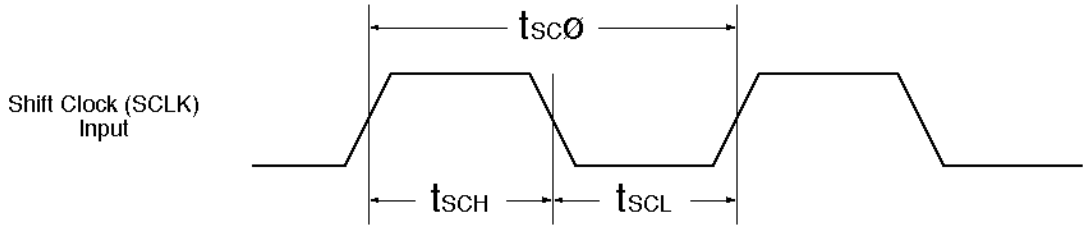


Figure 6. Shift Clock Pulse Width High and Pulse Width Low Timing Diagram

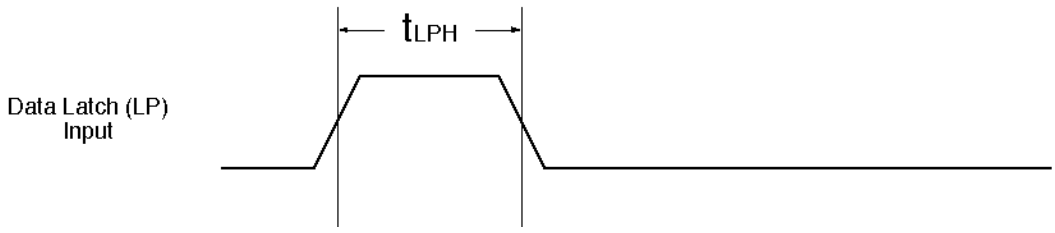


Figure 7. Data Latch Pulse Width High Timing Diagram

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

The main dc power is supplied to the part by these two connections. V_{DD} is the most-positive supply level and V_{SS} is ground.

VEE

This supply connection provides the negative power supply voltage for the common drivers.

VL1, VL3, VL4, VL6

These input pins are connected to the external voltage divider (See Figure 8).
Voltage supply level for the LCD :
VL1, VL6 : On-level of the LC
VL3, VL4 : Off-level of the LC

Data Latch (LP)

Display data (a complete line on display) is acknowledged by the falling edge of the LP signal.

Data Shift Clock (SCLK)

Input data (8 bit or 4 bit) is stored into a 8 bit / 4 bit data latch by the falling edge of SCLK.

Data Input (D0 to D7)

Data Input is either in 8 bit or 4 bit data bus format and is selectable by the DS input.

Data Format Select (DS)

This input is to select the data bus format. If set “Low”, the data bus format is 4-bit, if set “High”, the data bus format is 8-bit.

Left / Right Shift Select (L / $\overline{R}$)

This input pin provides the selection of the shift register operation (See Table 1).

L / $\overline{R}$ = “1”,	the data will shift left (LSB of the first input data will be loaded to SEG1).
L / $\overline{R}$ = “0”,	the data will shift right (LSB of the first input data will be loaded to SEG80).

Carry-In / Carry-Out ($\overline{EIO1}$ / $\overline{EIO2}$)

These two input / output pins perform the same function and depend on the shift register direction of operation. In right shift mode (L / $\overline{R}$ = “0”), the $\overline{EIO1}$ is the Carry-In input while the $\overline{EIO2}$ will be the Carry-Out output for cascading. In Left Mode (L / $\overline{R}$ = “1”), the pin functions and operation are reversed. (See Table 2)

Frame Signal Input (M)

This input signal is the frame sync. signal which provides an frame alternating output format of the segment output (See Figure 9).

M	0	0	1	1
Data	1	0	0	1
Output	VL1	VL3	VL4	VL6

Display-Off Enable ($\overline{DIS\text{-}OFF}$)

This input pin is active low. If set “LOW”, all output pins (Segment 1 to Segment 80) are forced to VL1.

Segment Output (Segment 1 to Segment 80)

These 80 output lines provide the high volt segment signal to the LCD panel. They are all at VL1 while display is turned off.

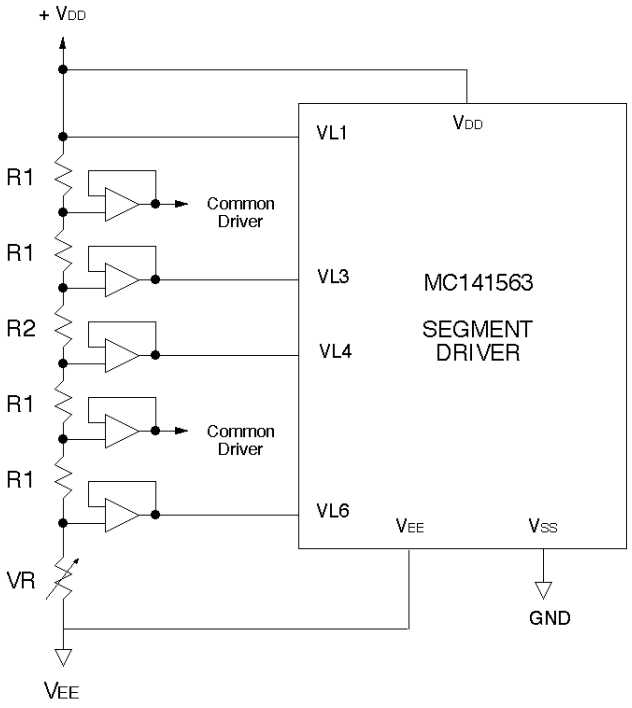


Figure 8. External Voltage Divider

L / $\overline{R}$	SCLK :	1	2	3	4	------	19	20
H	D0	01	05	09	13	------	73	77
	D1	02	06	10	14	------	74	78
	D2	03	07	11	15	------	75	79
	D3	04	08	12	16	------	76	80
L	D0	80	76	72	68	------	08	04
	D1	79	75	71	67	------	07	03
	D2	78	74	70	66	------	06	02
	D3	77	73	69	65	------	05	01

L / $\overline{R}$	SCLK	1	2	------	10
H	D0	01	09	------	73
	D1	02	10	------	74
	D2	03	11	------	75
	D3	04	12	------	76
	D4	05	13	------	77
	D5	06	14	------	78
	D6	07	15	------	79
	D7	08	16	------	80
L	D0	80	72	------	08
	D1	79	71	------	07
	D2	78	70	------	06
	D3	77	69	------	05
	D4	76	68	------	04
	D5	75	67	------	03
	D6	74	66	------	02
	D7	73	65	------	01

Table 1. Left / Right Shift Select and the Associated Data Bit Segment Output Mapping (a) 4 bit interface; (b) 8 bit interface

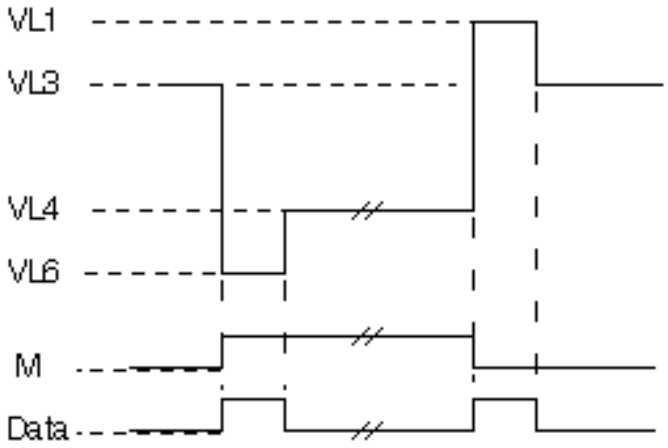


Figure 9. Data, M Inputs and Segment Output Format

L / $\overline{R}$	$\overline{EIO1}$	$\overline{EIO2}$
H	OUT	IN
L	IN	OUT

Table 2. Left / Right Shift Control and $\overline{EIO1}$, $\overline{EIO2}$ Relation

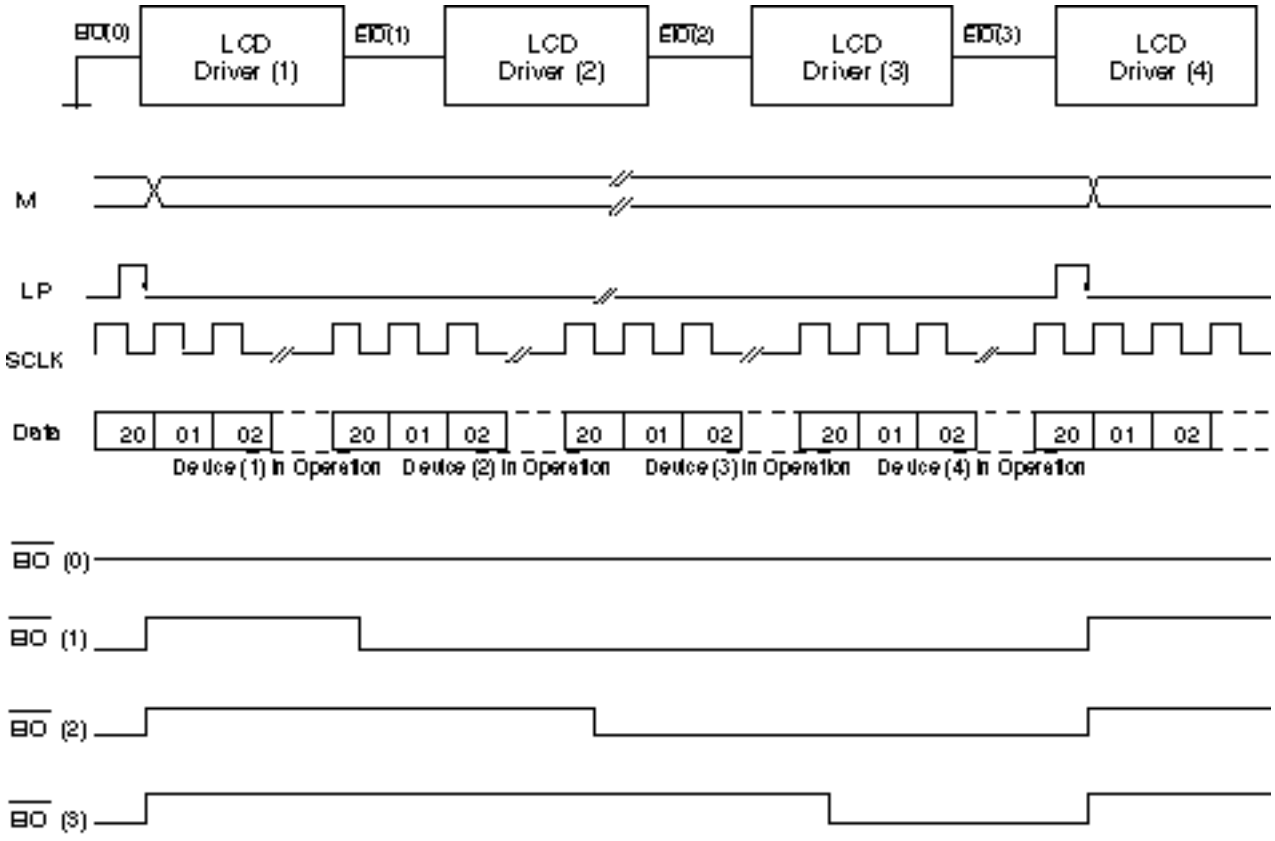


Figure 10. $\overline{EIO1}$ and $\overline{EIO2}$ in 4 Data Bit Application and Timing Diagram

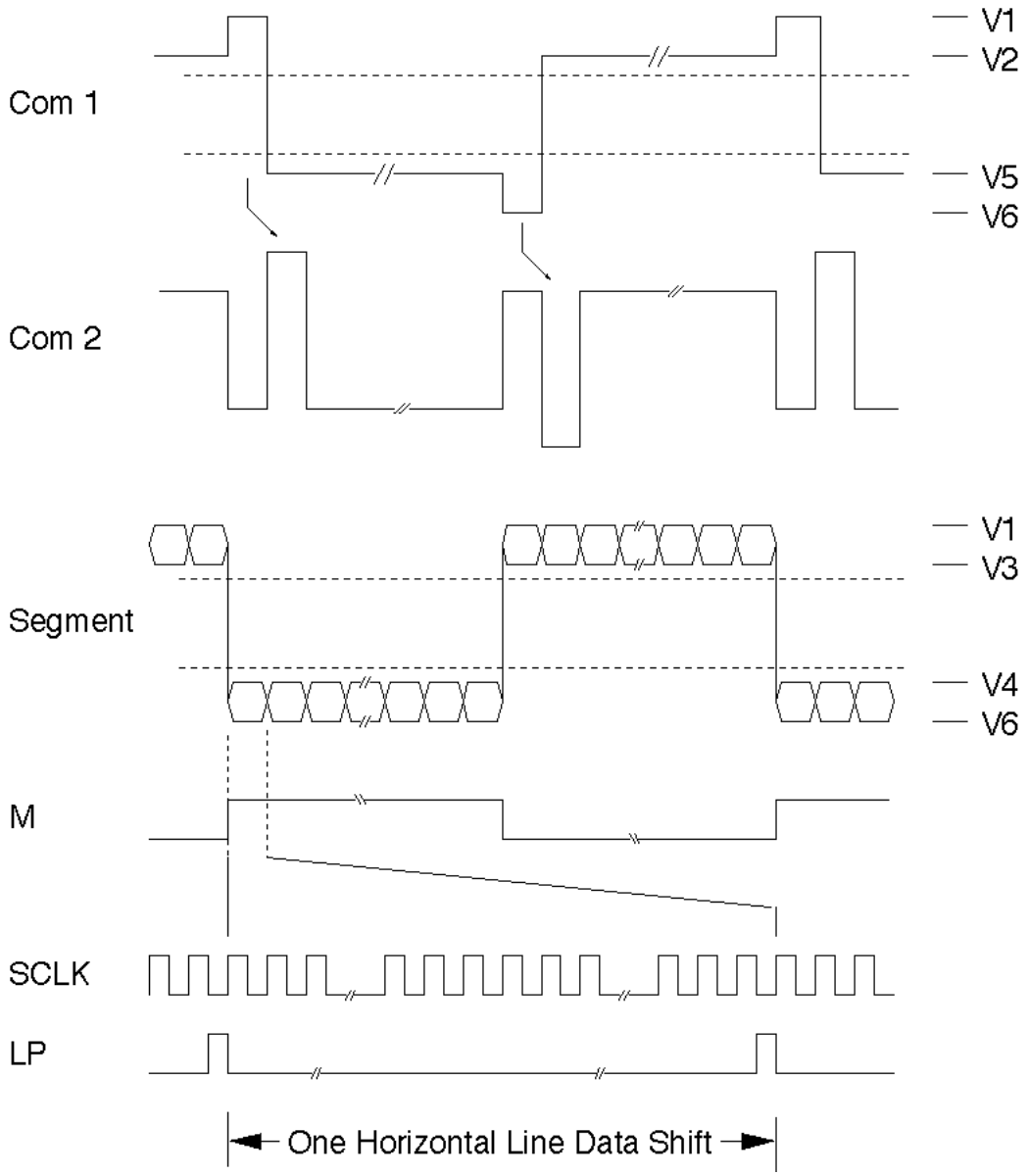
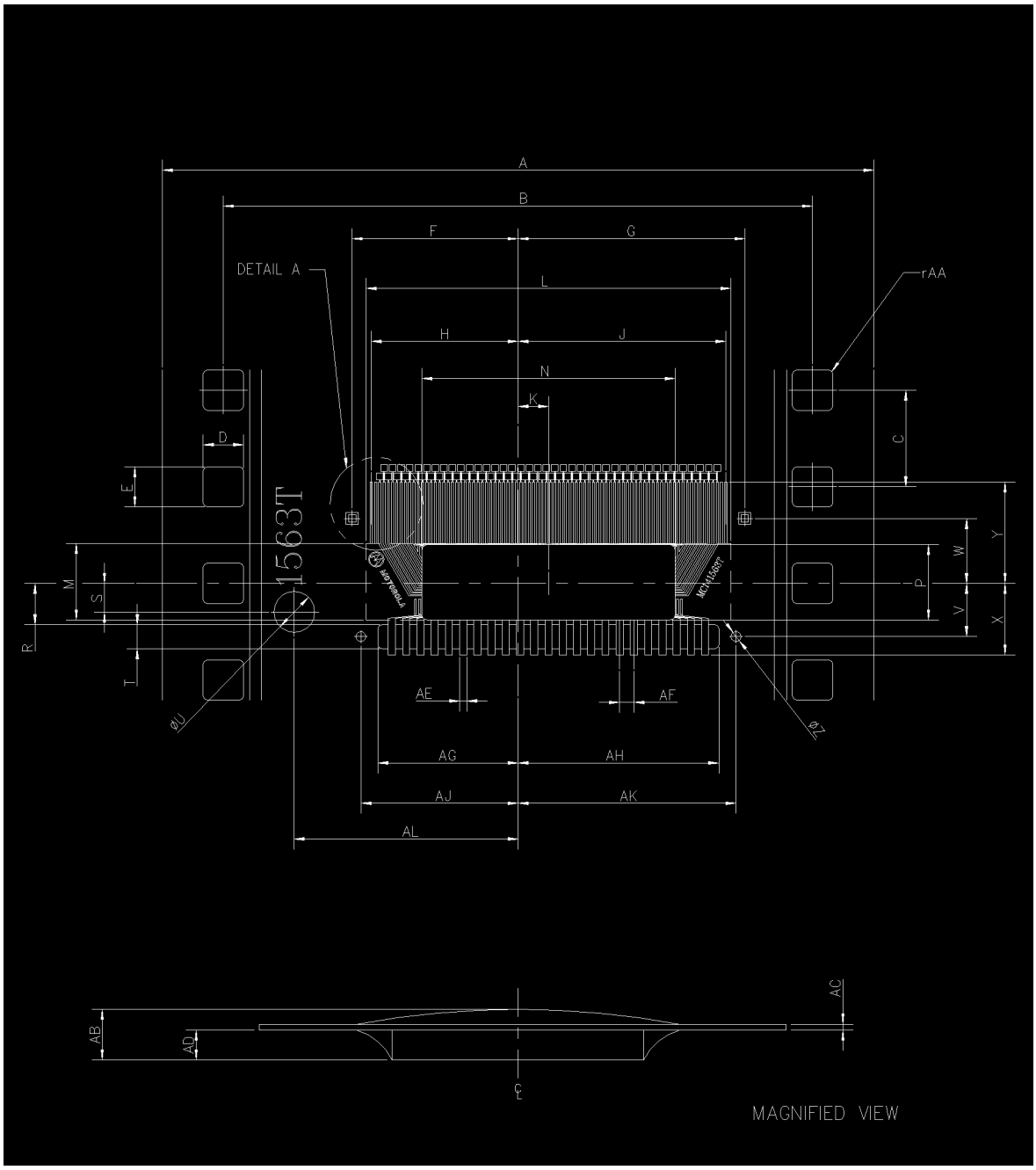


Figure 11. Common and Segment and Input Control Format Timing Diagram

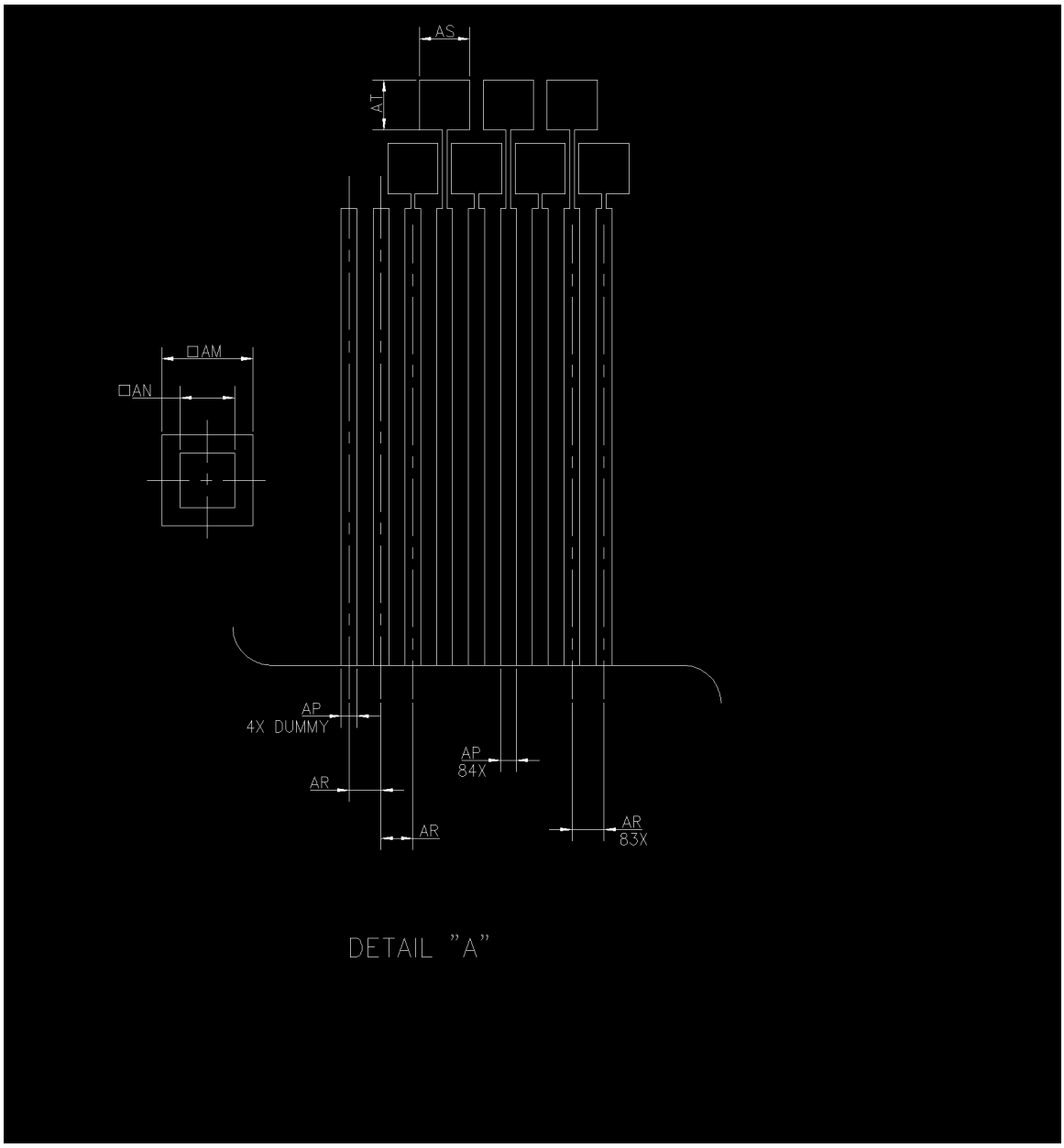
PACKAGE DIMENSIONS

MC141563T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



Reference : 98ASL00131A	Issue “0” released on 03/03/94

MC141563T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



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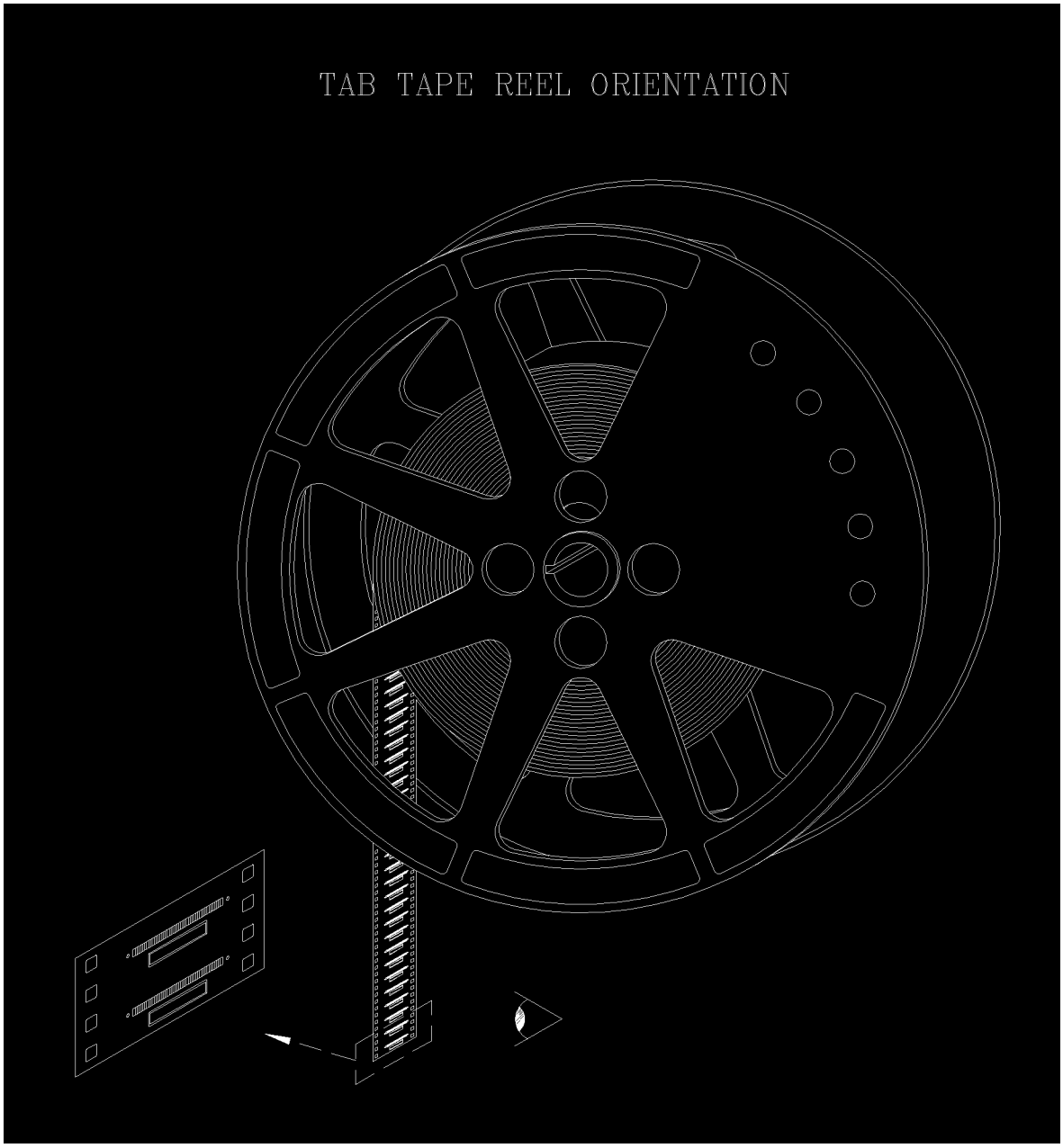
MC141563T TAB PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	**Min**	**Max**	**Min**	**Max**	**Dim**	**Min**	**Max**	**Min**	**Max**
A	34.775	35.175	1.3691	1.3848	AC	0.068	0.083	0.0027	0.0032
B	28.927	29.027	1.1389	1.1428	AD	0.579	0.629	0.0228	0.0248
C	4.720	4.780	0.1858	0.1882	AE	0.330	0.370	0.0130	0.0146
D	1.951	2.011	0.0768	0.0792	AF	0.690	0.710	0.0272	0.0280
E	1.951	2.011	0.0768	0.0792	AG	6.825	6.925	0.2687	0.2726
F	8.100	8.200	0.3189	0.3228	AH	9.825	9.925	0.3868	0.3907
G	11.100	11.200	0.4370	0.4409	AJ	7.675	7.775	0.3022	0.3061
H	7.201	7.229	0.2835	0.2846	AK	10.675	10.775	0.4203	0.4242
J	10.195	10.235	0.4014	0.4030	AL	10.500	11.500	0.4134	0.4528
K	1.000	2.000	0.0394	0.0787	AM	0.580	0.620	0.0228	0.0244
L	17.635	18.235	0.6943	0.7179	AN	0.340	0.380	0.0134	0.0150
M	3.490	4.090	0.1374	0.1610	AP	0.085	0.125	0.0033	0.0049
N	-	12.460	-	0.4906	AR	0.200	0.220	0.0079	0.0087
P	-	3.624	-	0.1427	AS	0.280	0.380	0.0110	0.0150
R	1.962	2.062	0.0772	0.0812	AT	0.280	0.380	0.0110	0.0150
S	0.900	1.900	0.0354	0.0748					
T	1.150	1.250	0.0453	0.0492					
U	1.950	2.050	0.0768	0.0807					
V	2.562	2.662	0.1009	0.1048					
W	3.146	3.246	0.1239	0.1278					
X	3.462	3.562	0.1363	0.1402					
Y	4.938	5.038	0.1944	0.1983					
Z	0.450	0.550	0.0177	0.0217					
AA	-	0.200	-	0.0079					
AB	0.686	0.838	0.0270	0.0330					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper Thickness: 1/2 oz.
4. Tin plating thickness: 0.4µm
5. 2 sprocket hole device

Reference : 98ASL00131A	Issue “0” released on 03/03/94

MC141563T



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Application Example

320 x 300